TMP61 ±1% 10-kΩ Linear Thermistor With 0402 and 0603 Package Options

1 Features

- Silicon-based thermistor with a positive temperature coefficient (PTC)
- Linear resistance change across temperature
- 10-kΩ nominal resistance at 25°C (R25)
  - ±1% maximum (0°C to 70°C)
- Wide operating temperature of –40°C to +150 °C
- Consistent sensitivity across temperature
  - 6400 ppm/°C TCR (25°C)
  - 0.2% typical TCR tolerance across temperature range
- Fast thermal response time of 0.6 s (DEC)
- Long lifetime and robust performance
  - Built-in fail-safe in case of short-circuit failures
  - 0.5% typical long term sensor drift

2 Applications

- Temperature monitoring
  - HVAC and thermostats
  - Industrial control and appliances
- Thermal compensation
  - Display backlights
  - Building automation
- Thermal threshold detection
  - Motor control
  - Chargers

3 Description

Get started today with the Thermistor Design Tool, offering complete resistance vs temperature table (R-T table) computation, other helpful methods to derive temperature and example C-code.

The TMP61 linear thermistor offers linearity and consistent sensitivity across temperature to enable simple and accurate methods for temperature conversion. The low power consumption and a small thermal mass of the device minimize self-heating.

With built-in fail-safe behaviors at high temperatures and powerful immunity to environmental variation, these devices are designed for a long lifetime of high performance. The small size of the TMP6 series also allows for close placement to heat sources and quick response times.

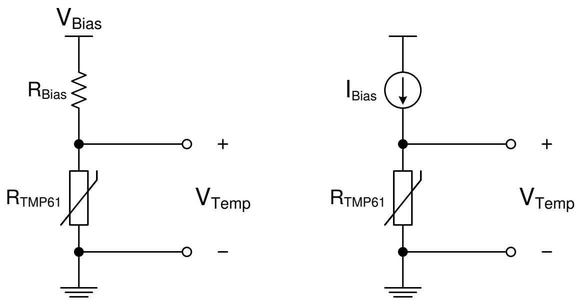
Take advantage of benefits over NTC thermistors such as no extra linearization circuitry, minimized calibration, less resistance tolerance variation, larger sensitivity at high temperatures, and simplified conversion methods to save time and memory.

The TMP61 is currently available in a 0402 X1SON package, a 0603 SOT-5X3 package, and a 2-pin through-hole TO-92S package.

Package Information

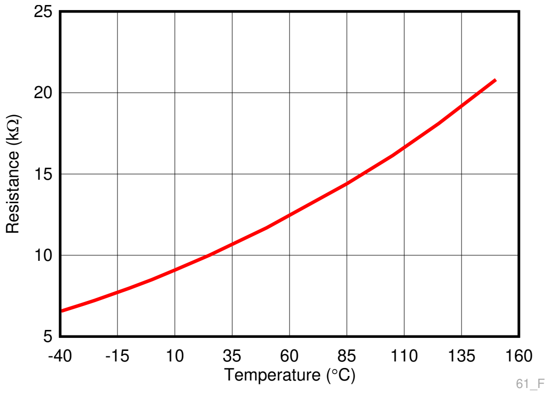
PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
TMP61	DEC (X1SON, 2)	1.00 mm × 0.60 mm
	LPG (TO-92S, 2)	4.00 mm × 1.52 mm
	DYA (SOT-5X3, 2)	1.60 mm × 0.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



$$V_{Temp} = \frac{V_{Bias} * R_{TMP61}}{R_{Bias} + R_{TMP61}} \qquad V_{Temp} = I_{Bias} * R_{TMP61}$$

Typical Implementation Circuits



Typical Resistances vs Ambient Temperature

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4 Device Comparison

Table 4-1. Device Comparison

PART NUMBER	R25 TYP	R25 %TOL	RATING	T_A	PACKAGE OPTIONS
TMP61	10k	1%	Catalog	–40°C to 125°C	X1SON / DEC (0402)
				–40°C to 150°C	SOT-5X3 / DYA (0603)
				–40°C to 150°C	TO-92S / LPG
TMP61-Q1	10k	1%	Automotive Grade-1	–40°C to 125°C	X1SON / DEC (0402)
			Automotive Grade-0	–40°C to 150°C	SOT-5X3 / DYA (0603)
				–40°C to 170°C	TO-92S / LPG
TMP63	100k	1%	Catalog	–40°C to 125°C	X1SON / DEC (0402)
				–40°C to 150°C	SOT-5X3 / DYA (0603)
TMP63-Q1	100k	1%	Automotive Grade-1	–40°C to 125°C	X1SON / DEC (0402)
			Automotive Grade-0	–40°C to 150°C	SOT-5X3 / DYA (0603)
TMP64	47k	1%	Catalog	–40°C to 125°C	X1SON / DEC (0402)
				–40°C to 150°C	SOT-5X3 / DYA (0603)
TMP64-Q1	47k	1%	Automotive Grade-1	–40°C to 125°C	X1SON / DEC (0402)
			Automotive Grade-0	–40°C to 150°C	SOT-5X3 / DYA (0603)

5 Pin Configuration and Functions

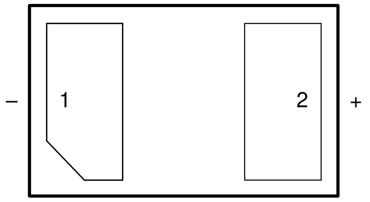
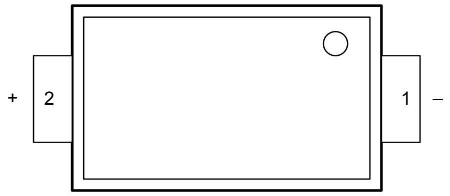
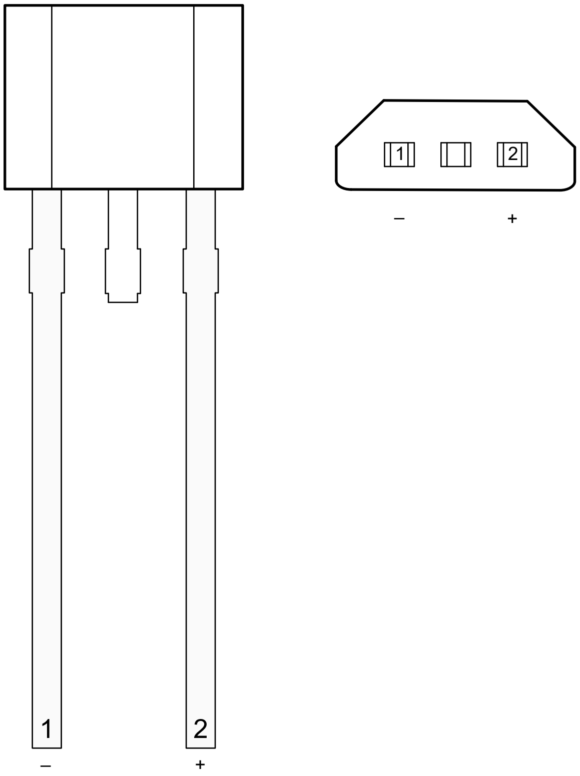


Figure 5-1. DEC Package 2-Pin X1SON Top View



ID mark is identified as a dot in the ID area and it denotes pin 1.

Figure 5-2. DYA Package 2-Pin SOT-5X3 Top View



Front view is described as chamfers of TO-92S facing the user. Bottom view is described as pins coming out of the page.

Figure 5-3. LPG Package 2-Pin TO-92S Front View, Bottom View

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
–	1	—	Thermistor (–) and (+) terminals. For proper operation, ensure a positive bias where the + terminal is at a higher voltage potential than the – terminal.
+	2		

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Voltage across the device		6	V
Junction temperature (T_J)	–65	155	°C
Current through the device		450	µA
Storage temperature (T_{stg})	–65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM) per JESD22-A114(1)	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{Sns}	Voltage Across Pins 2 (+) and 1 (–)	0		5.5	V
I_{Sns}	Current passing through the device	0		400	µA
T_A	Operating free-air temperature (X1SON/DEC Package)	–40		125	°C
	Operating free-air temperature (TO-92S/LPG Package)	–40		150	
	Operating free-air temperature (SOT-5X3/DYA Package)	–40		150	

6.4 Thermal Information

THERMAL METRIC(1) (2)		TMP61			UNIT
		DEC (X1SON)	LPG (TO-92S)	DYA (SOT-5X3)	
		2 PINS	2 PINS	2 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(3) (4)	443.4	215	742.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	195.7	99.9	315.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	254.6	191.7	506.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.9	35.1	109.3	°C/W
Y_{JB}	Junction-to-board characterization parameter	254.5	191.7	500.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) For information on self-heating and thermal response time see Layout Guidelines section.
(3) The junction to ambient thermal resistance ($R\theta_{JA}$) under natural convection is obtained in a simulation on a JEDEC-standard, High-K board as specified in JESD51-7, in an environment described in JESD51-2. Exposed pad packages assume that thermal vias are included in the PCB, per JESD 51-5.
(4) Changes in output due to self heating can be computed by multiplying the internal dissipation by the thermal resistance.

6.5 Electrical Characteristics

T_A = –40°C to 150 °C, I_{Sns} = 200 µA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{25}	Thermistor Resistance at 25°C[1]	T_A = 25°C	9.9	10	10.1	kΩ
R_{TOL}	Resistance Tolerance[1]	T_A = 25°C	–1		1	%
R_{TOL}	Resistance Tolerance[1]	T_A = 0°C to 70°C	–1		1	%
		T_A = –40°C to 150°C	–1.5		1.5	
TCR_{-35}	Temperature Coefficient of Resistance	T1 = –40°C, T2 = –30°C		+6220		ppm/°C
TCR_{25}		T1 = 20°C, T2 = 30°C		+6400		
TCR_{85}		T1 = 80°C, T2 = 90°C		+5910		
TCR_{-35} %	Temperature Coefficient of Resistance Tolerance	T1 = –40°C, T2 = –30°C		±0.4		%
TCR_{25} %		T1 = 20°C, T2 = 30°C		±0.2		
TCR_{85} %		T1 = 80°C, T2 = 90°C		±0.3		
ΔR	Sensor Long Term Drift (Reliability)	96 hours continuous operation RH = 85 %, T_A = 130°C, V_{Bias} = 5.5V	-1	0.1	1	%
		600 hours continuous operation at T_A = 150°C V_{Bias} = 5.5V, DEC Package	-1	0.5	1.8	
		600 hours continuous operation at T_A = 150 °C V_{Bias} = 5.5V, DYA Package	-1	0.2	1.2	
		1000 hours continuous operation at T_A = 150 °C V_{Bias} = 5.5V, DYA Package	-1	0.2	1.2	
		1000 hours continuous operation at T_A = 150°C V_{Bias} = 5.5V, LPG Package	-0.5	0.5	1.4	
$t_{RES\ (stirred\ liquid)}$	Thermal response to 63 % (DEC Package)	T1 = 25°C in Still Air to T2 = 125°C in Stirred Liquid		0.6		s
$t_{RES\ (stirred\ liquid)}$	Thermal response to 63 % (LPG Package)	T1 = 25°C in Still Air to T2 = 125°C in Stirred Liquid		2.9		s
$t_{RES\ (still\ air)}$	Thermal response to 63 % (DEC Package)	T1 = 25°C to T2 = 70°C in Still Air		3.2		s
$t_{RES\ (still\ air)}$	Thermal response to 63 % (LPG Package)	T1 = 25°C to T2 = 70°C in Still Air		20		s

(1) Limits defined based on 4th order equation, tolerance will change with 'Sensor Long Term Drift' specification.

6.6 Typical Characteristics

at T_A = 25°C, (unless otherwise noted)

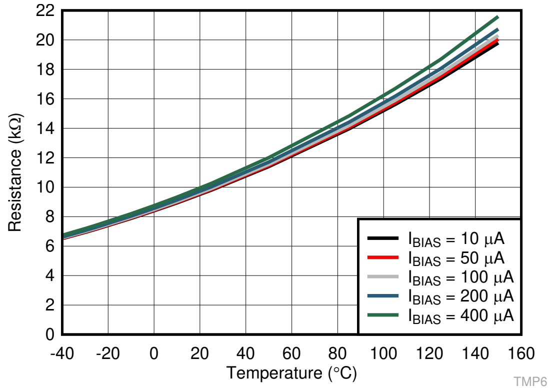
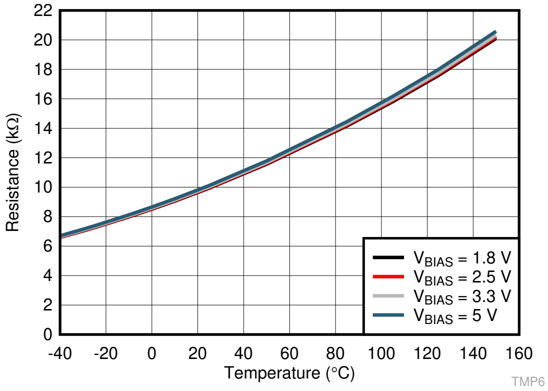


Figure 6-1. Resistance vs Ambient Temperature Using Multiple Bias Currents



R_{BIAS} = 10 kΩ with ±0.01% tolerance

Figure 6-2. Resistance vs Ambient Temperature Using Multiple Bias Voltages

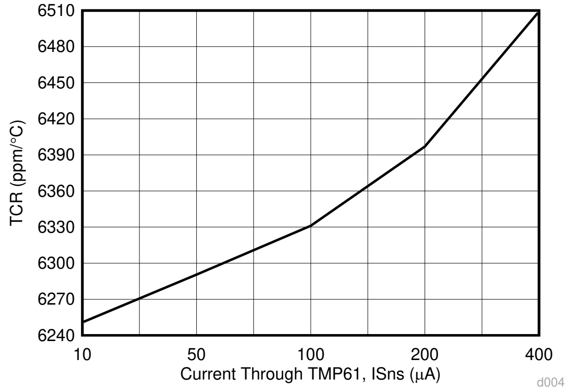
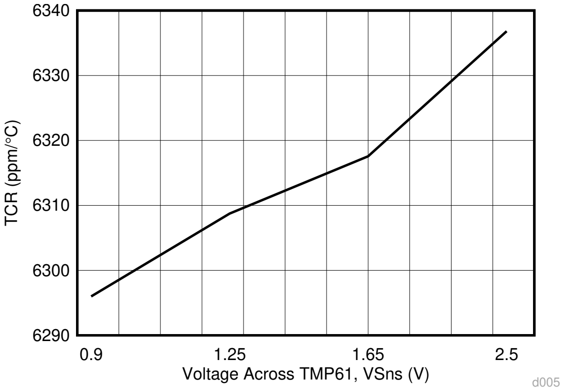


Figure 6-3. TCR vs Sense Currents (I_{SNS})



V_{Sns} = 1.8 V, 2.5 V, 3.3 V, and 5.0 V, R_{Bias} = 10 kΩ with ±0.01% Tolerance

Figure 6-4. TCR vs Sense Voltages, V_{Sns}

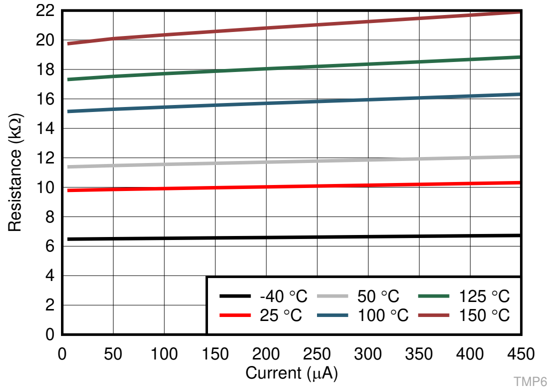
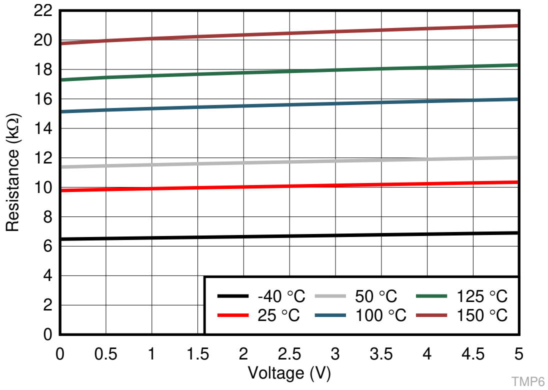
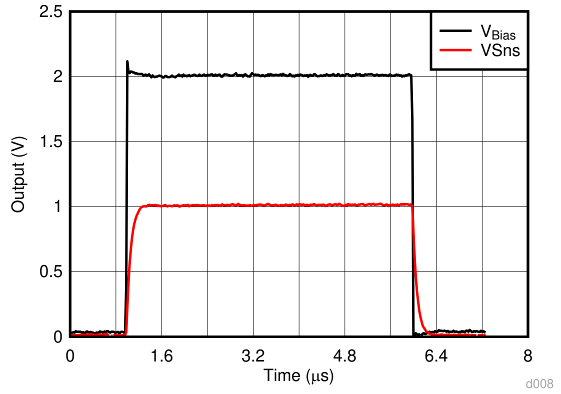


Figure 6-5. Supply Dependence Resistance vs Bias Current



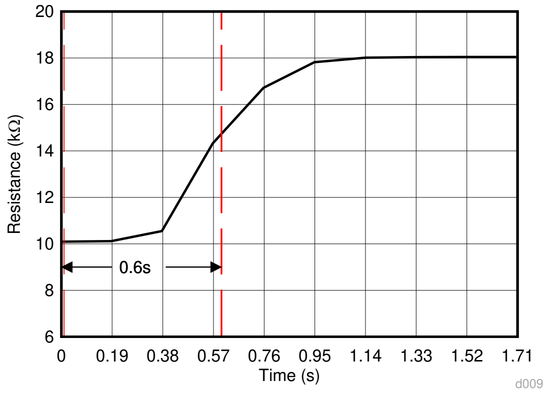
R_{Bias} = 10 kΩ (±0.01% tolerance)

Figure 6-6. Supply Dependence vs Bias Voltage



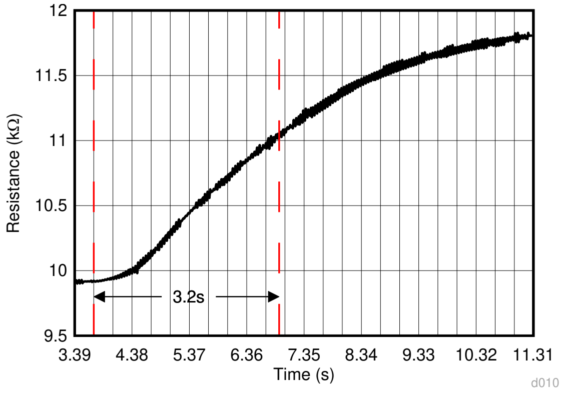
V_{SNS} = 1 V

Figure 6-7. Step Response



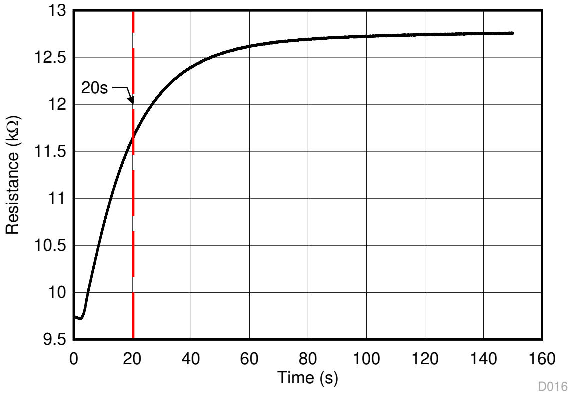
Ambient material: stirred liquid

Figure 6-8. Thermal Response Time (DEC package)



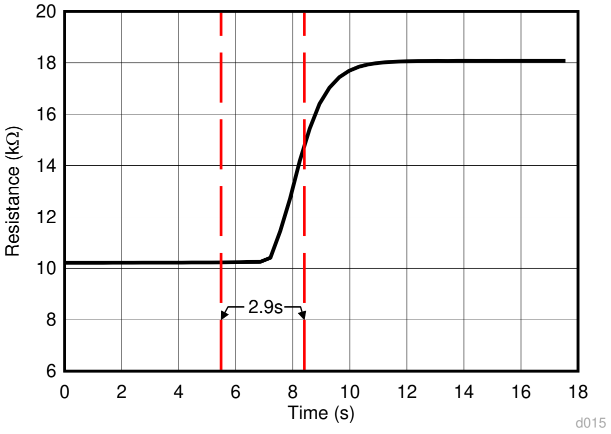
Ambient condition: still air

Figure 6-9. Thermal Response Time (DEC and DYA Package)



Ambient condition: still air

Figure 6-10. Thermal Response Time (LPG Package)



Ambient material: stirred liquid

Figure 6-11. Thermal Response Time (LPG Package)

7 Detailed Description

7.1 Overview

The TMP61 silicon linear thermistor has a linear positive temperature coefficient (PTC) that results in a uniform and consistent temperature coefficient resistance (TCR) across a wide operating temperature range. TI uses a special silicon process where the doping level and active region areas devices control the key characteristics (the temperature coefficient resistance (TCR) and nominal resistance (R25)). The device has an active area and a substrate due to the polarized terminals. Connect the positive terminal to the highest voltage potential. Connect the negative terminal to the lowest voltage potential.

Unlike an NTC, which is a purely resistive device, the TMP61 resistance is affected by the current across the device and the resistance changes when the temperature changes. In a voltage divider circuit, TI recommends to maintain the top resistor value at 10 kΩ. Changing the top resistor value or the V_{BIAS} value changes the resistance vs temperature table (R-T table) of the TMP61, and subsequently the polynomials as described in the *Design Requirements* section. Consult the *TMP61 R-T table* section for more information.

Equation 1 can help the user approximate the TCR.

$$\mathrm{TCR} = \frac{\left(R_{T2} - R_{T1}\right)}{\left(T2 - T1\right) \times R_{\frac{(T2-T1)}{2}}} \tag{1}$$

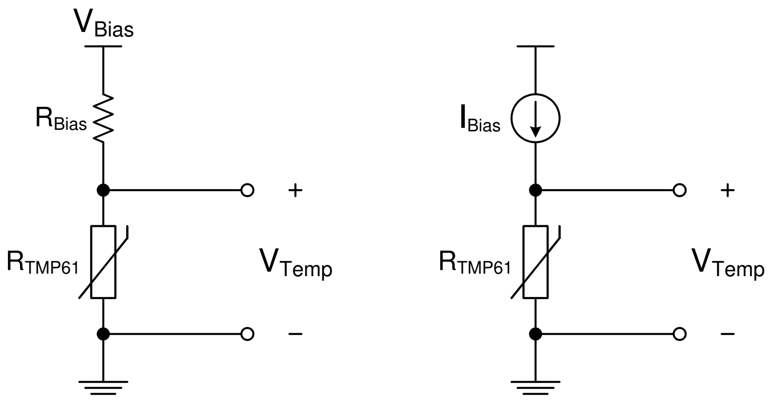
where

- TCR is in ppm/°C

Key terms and definitions:

- I_{SNS}: Current flowing through the TMP61 device
- V_{SNS}: Voltage across the two TMP61 terminal
- I_{BIAS}: Current supplied by the biasing circuit.
- V_{BIAS}: Voltage supplied by the biasing circuit.
- V_{TEMP}: Output voltage that corresponds to the measured temperature. Note that this is different from V_{SNS}. In the use case of a voltage divider circuit with the TMP61 in the high side, V_{TEMP} is measured across R_{BIAS}.

7.2 Functional Block Diagram



$$V_{Temp} = \frac{V_{Bias} * R_{TMP61}}{R_{Bias} + R_{TMP61}} \qquad V_{Temp} = I_{Bias} * R_{TMP61}$$

Figure 7-1. Typical Implementation Circuits

7.3 Feature Description

7.3.1 TMP61 R-T table

The TMP61 R-T table must be re-calculated for any change in the bias voltage, bias resistor, or bias current. TI provides a Thermistor Design Tool to calculate the R-T table. The system designer must always validate the calculations provided.

7.3.2 Linear Resistance Curve

The TMP61 has good linear behavior across the whole temperature range as shown in *Typical Characteristics*. This range allows a simpler resistance-to-temperature conversion method that reduces look-up table memory requirements. The linearization circuitry or midpoint calibration associated with traditional NTCs is not necessary with the device.

The linear resistance across the entire temperature range allows the device to maintain sensitivity at higher operating temperatures.

7.3.3 Positive Temperature Coefficient (PTC)

The TMP61 has a positive temperature coefficient. As temperature increases the device resistance increases leading to a reduction in power consumption of the bias circuit. In comparison, a negative coefficient system increases power consumption with temperature as the resistance decreases.

The TMP61 benefits from the reduced power consumption of the bias circuit with less self-heating than a typical NTC system.

7.3.4 Built-In Fail Safe

The TMP6 family feature a positive temperature coefficient. During a short-to-supply condition, the thermistor will have increased current and power dissipated. Due to the positive temperature slope, the TMP6 will increase resistance and limit self-heating by design.

In contrast, a NTC would continually reduce resistance due to self-heating leading to a positive feedback of increasing power dissipation and decreasing resistance.

7.4 Device Functional Modes

The device operates in only one mode when operated within the *Recommended Operating Conditions*.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TMP61 is a positive temperature coefficient (PTC) linear silicon thermistor. The device behaves as a temperature-dependent resistor, and may be configured in a variety of ways to monitor temperature based on the system-level requirements. The TMP61 has a nominal resistance at 25°C (R25) of 9.82 10 kΩ with ±1% maximum tolerance, a maximum operating voltage of 5.5 V (V_{SNS}), and maximum supply current of 400 µA (I_{SNS}). This device may be used in a variety of applications to monitor temperature close to a heat source with the very small DEC package option compatible with the typical 0402 (inch) footprint. Some of the factors that influence the total measurement error include the ADC resolution (if applicable), the tolerance of the bias current or voltage, the tolerance of the bias resistance in the case of a voltage divider configuration, and the location of the sensor with respect to the heat source.

8.2 Typical Application

8.2.1 Thermistor Biasing Circuits

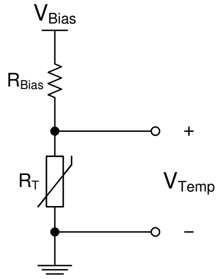


Figure 8-1. Voltage Biasing Circuit With Linear Thermistor

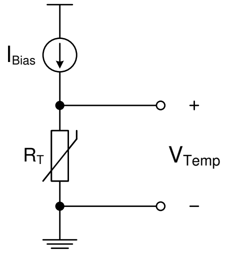


Figure 8-2. Current Biasing Circuit With Linear Thermistor

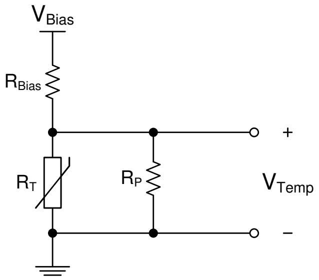


Figure 8-3. Voltage Biasing Circuit With Non-Linear Thermistor

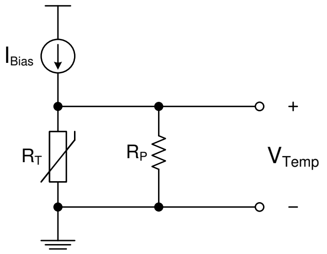


Figure 8-4. Current Biasing Circuit With Non-Linear Thermistor

8.2.1.1 Design Requirements

Existing thermistors, in general, have a non-linear temperature versus resistance curve. To linearize the thermistor response, the engineer can use a voltage linearization circuit with a voltage divider configuration, or a resistance linearization circuit by adding another resistance in parallel with the thermistor, R_P. The *Thermistor Biasing Circuits* section highlights the two implementations where R_T is the thermistor resistance. To generate an output voltage across the thermistor, the engineer can use a voltage divider circuit with the thermistor placed at either the high side (close to supply) or low side (close to ground), depending on the desired voltage response (negative or positive). Alternatively, the resistor can be biased directly using a precision current source (yielding the highest accuracy and voltage gain). It is common to use a voltage divider with thermistors because of its simple implementation and lower cost. The TMP61, on the other hand, has a linear positive temperature coefficient (PTC) of resistance such that the voltage measured across it increases linearly with temperature. As such, the need for linearization circuits is no longer a requirement, and a simple current source or a voltage divider circuit can be used to generate the temperature voltage.

This output voltage can be interpreted using a comparator against a voltage reference to trigger a temperature trip point that is either tied directly to an ADC to monitor temperature across a wider range or used as feedback input for an active feedback control circuit.

The voltage across the device, as described in Equation 2, can be translated to temperature using either a lookup table method (LUT) or a fitting polynomial, V(T). The Thermistor Design Tool must be used to translate Vtemp to Temperature. The temperature voltage must first be digitized using an ADC. The necessary resolution of this ADC is dependent on the biasing method used. Additionally, for best accuracy, tie the bias voltage (V_{BIAS}) to the reference voltage of the ADC to create a measurement where the difference in tolerance between the bias voltage and the reference voltage cancels out. The application can also include a low-pass filter to reject system level noise. In this case, place the filter as close to the ADC input as possible.

8.2.1.2 Detailed Design Procedure

The resistive circuit divider method produces an output voltage (V_{TEMP}) scaled according to the bias voltage (V_{BIAS}). When V_{BIAS} is also used as the reference voltage of the ADC, any fluctuations or tolerance error due to the voltage supply are cancelled and do not affect the temperature accuracy (as shown in Figure 8-5). Use Equation 2 to calculate the output voltage (V_{TEMP}) based on the variable resistance of the TMP61 (R_{TMP61}) and bias resistor (R_{BIAS}). Use Equation 3 to calculate the ADC code that corresponds to that output voltage, ADC full-scale range, and ADC resolution.

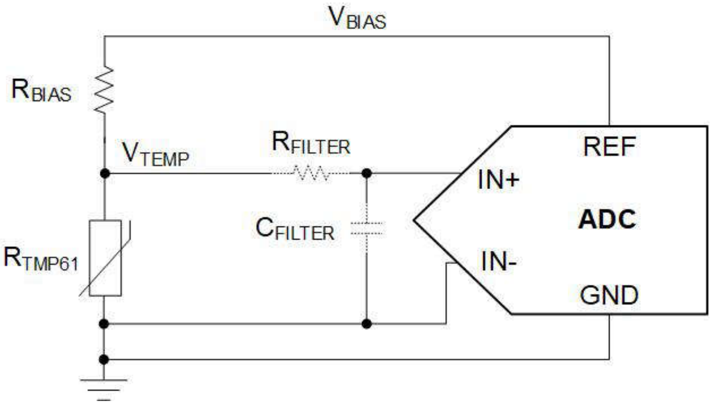


Figure 8-5. TMP61 Voltage Divider With an ADC

$$V_{TEMP} = V_{BIAS} \times \left(\frac{R_{TMP61}}{R_{TMP61} + R_{BIAS}} \right) \tag{2}$$

$$\text{ADC Code} = \frac{V_{TEMP}}{FSR} 2^n \tag{3}$$

where

- FSR is the full-scale range of the ADC, which is the voltage at REF to GND (V_{REF})
- n is the resolution of the ADC

Equation 4 shows when $V_{REF} = V_{BIAS}$, V_{BIAS} cancels out.

$$\text{ADC Code} = \frac{V_{BIAS} \times \left(\frac{R_{TMP61}}{R_{TMP61} + R_{BIAS}}\right)}{V_{BIAS}} 2^n = \left(\frac{R_{TMP61}}{R_{TMP61} + R_{BIAS}}\right) 2^n \tag{4}$$

Use a polynomial equation or a LUT to extract the temperature reading based on the ADC code read in the microcontroller. Use the Thermistor Design Tool to translate the TMP61 resistance to temperature.

The cancellation of V_{BIAS} is one benefit to using a voltage-divider (ratiometric approach), but the sensitivity of the output voltage of the divider circuit cannot increase much. Therefore, this application design does not use all of the ADC codes due to the small voltage output range compared to the FSR. This application is very common, however, and is simple to implement.

A current source-based circuit, such as the one shown in Figure 8-6, offers better control over the sensitivity of the output voltage and achieve higher accuracy. In this case, the output voltage is simply V = I × R. For example, if a current source of 40 µA is used with the device, the output voltage spans approximately 5.5 V and has a gain up to 40 mV/°C. Having control over the voltage range and sensitivity allows for full use of the ADC codes and full-scale range. Figure 8-7 shows the temperature voltage for various bias current conditions. Similar to the ratiometric approach, if the ADC has a built-in current source that shares the same bias as the reference voltage of the ADC, the tolerance of the supply current cancels out. In this case, a precision ADC is not required. This method yields the best accuracy, but can increase the system implementation cost.

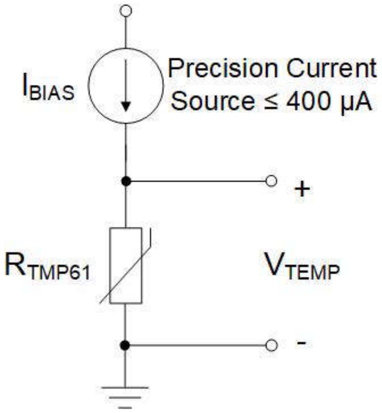


Figure 8-6. TMP61 Biasing Circuit With Current Source

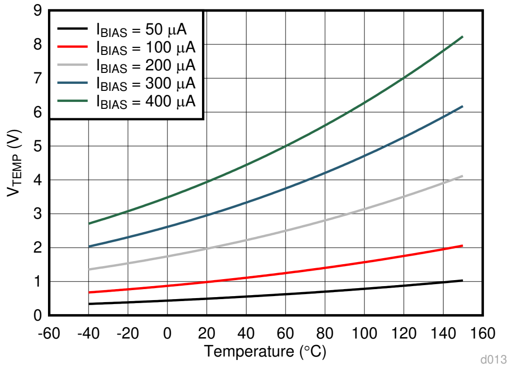


Figure 8-7. TMP61 Temperature Voltage With Varying Current Sources

In comparison to the non-linear NTC thermistor in a voltage divider, the TMP61 has an enhanced linear output characteristic. The two voltage divider circuits with and without a linearization parallel resistor, R_P, are shown in Figure 8-8. Consider an example where V_{BIAS} = 5 V, R_{BIAS} = 100 kΩ, and a parallel resistor (R_P) is used with the NTC thermistor (R_{NTC}) to linearize the output voltage with an additional 100-kΩ resistor. The output characteristics of the voltage dividers are in Figure 8-9. The device produces a linear curve across the entire temperature range while the NTC curve is only linear across a small temperature region. When the parallel resistor (R_P) is added to the NTC circuit, the added resistor makes the curve much more linear but greatly affects the output voltage range.

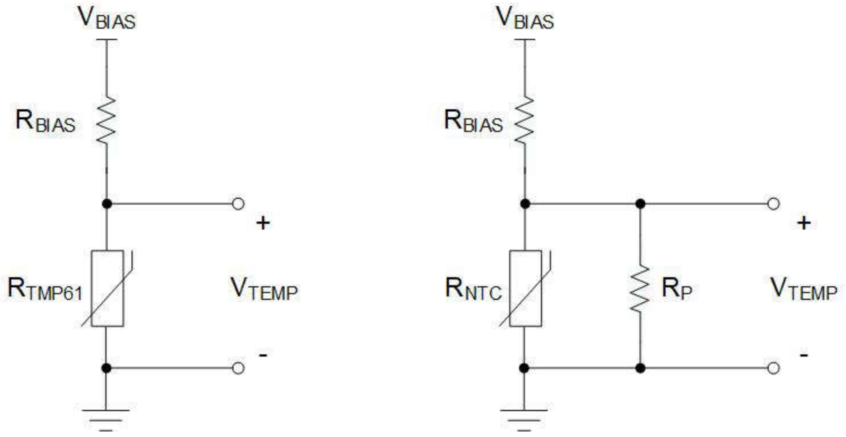


Figure 8-8. TMP61 vs NTC With Linearization Resistor (R_P) Voltage Divider Circuits

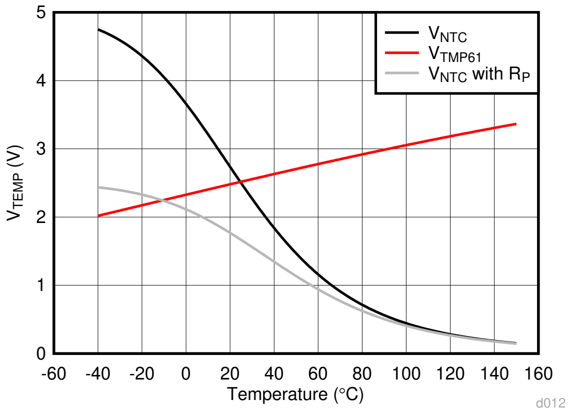


Figure 8-9. NTC With and Without a Linearization Resistor vs TMP61 Temperature Voltages

8.2.1.2.1 Thermal Protection With Comparator

Use the TMP61 device along with a voltage reference, and a comparator to program the thermal protection. As shown in Figure 8-10, the output of the comparator remains low until the voltage of the thermistor divider, with R_{BIAS} and R_{TMP61}, rises above the threshold voltage set by R_1 and R_2. When the output goes high, the comparator signals an overtemperature warning signal. The engineer can also program the hysteresis to prevent the output from continuously toggling around the temperature threshold when the output returns low. Either a comparator with built-in hysteresis or feedback resistors may be used.

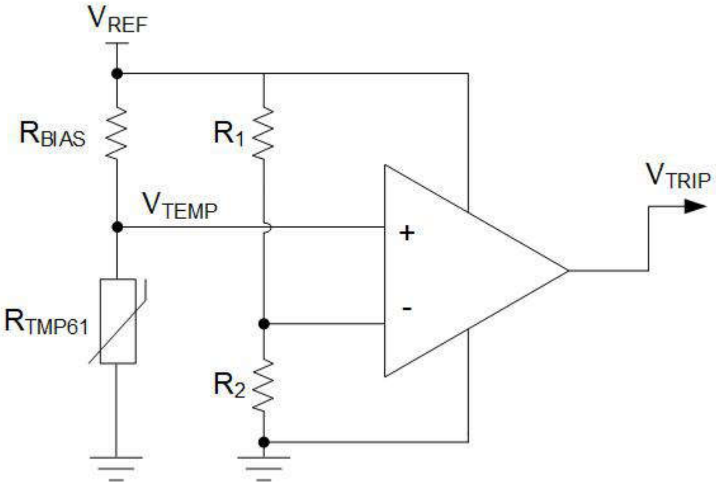


Figure 8-10. Temperature Switch Using TMP61 Voltage Divider and a Comparator

8.2.1.2.2 Thermal Foldback

One application that uses the output voltage of the TMP61 in an active control circuit is thermal foldback. This is performed to reduce, or fold back, the current driving a string of LEDs, for example. At high temperatures, the LEDs begin to heat up due to environmental conditions and self heating. Thus, at a certain temperature threshold based on the LED's safe operating area, the driving current must be reduced to cool down the LEDs and prevent thermal runaway. The device voltage output increases with temperature when the output is in the lower position of the voltage divider and can provide a response used to fold back the current. Typically, the device holds the current at a specified level until a high temperature is reached, known as the knee point, at which the current must be rapidly reduced in order to continue operation. To better control the temperature/voltage sensitivity, the device uses a rail-to-rail operational amplifier. Figure 8-11 shows the temperature knee point where the foldback begins. The set by the reference voltage (2.5 V) at the positive input, and the feedback resistors set the response of the foldback curve. The foldback knee point may be chosen based on the output of the voltage divider and the corresponding temperature from Equation 5 (110°C, for example). The device uses a buffer between the voltage divider with R_{TMP61} and the input to the op amp to prevent loading and variations in V_{TEMP}.

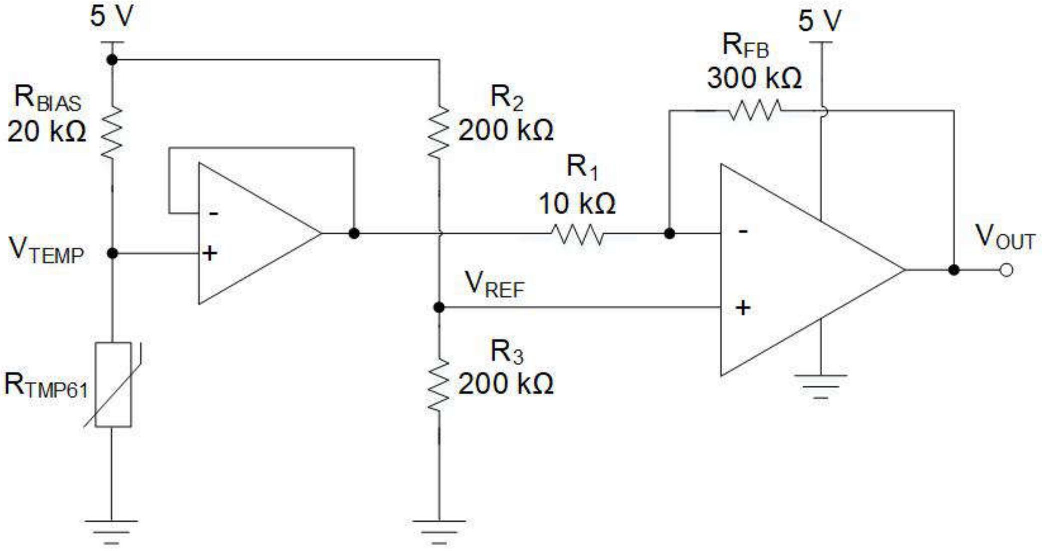


Figure 8-11. Thermal Foldback Using TMP61 Voltage Divider and a Rail-to-Rail Op Amp

The op amp remains high as long as the voltage output is below V_{REF}. When the temperature goes above 110°C, the output falls to the 0-V rail of the op amp. The rate at which the foldback occurs depends on the feedback network, R_{FB} and R_1, which varies the gain of the op amp, G, as shown in Equation 6. The foldback behavior controls the voltage and temperature sensitivity of the circuit. The device feeds this voltage output into a LED driver circuit that adjusts output current accordingly. V_{OUT} is the final output voltage used for thermal foldback and is calculated in Equation 7. Figure 8-12 describes the output voltage curve in this example which sets the knee point at 110°C.

$$V_{TEMP} = V_{BIAS} \times \left(\frac{R_{TMP61}}{R_{TMP61} + R_{BIAS}} \right) \tag{5}$$

$$G = \frac{R_{FB}}{R_1} \tag{6}$$

$$V_{OUT} = -G \times V_{TEMP} + (1 + G) \times V_{REF} \tag{7}$$

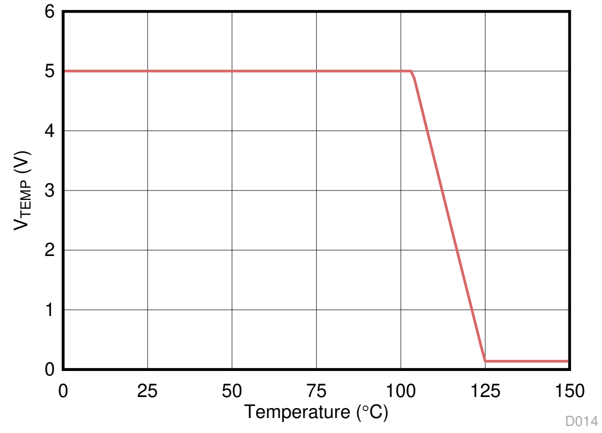


Figure 8-12. Thermal Foldback Voltage Output Curve

8.2.1.3 Application Curve

The TMP61 accuracy varies depending on the selected biasing circuit. This variation can be seen in Figure 8-13. V_{TEMP} is shown with either V_{BIAS} at 2 V in a resistor divider circuit (R_{BIAS} = 10 kΩ ±1%) or I_{BIAS} at 200 µA. Supply sources used are assumed to be ideal. The best accuracy is achieved using a direct current bias method.

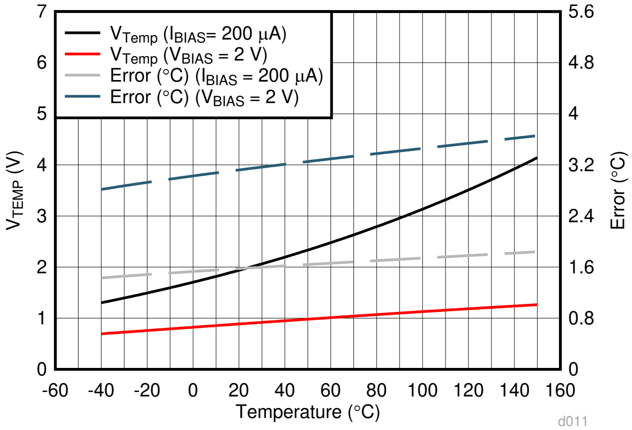


Figure 8-13. TMP61 Voltage Output and Temperature Error Based on the Bias Method

8.3 Power Supply Recommendations

The maximum recommended operating voltage of the TMP61 is 5.5 V (V_{SNS}), and the maximum current through the device is 400 µA (I_{SNS}).

8.4 Layout

8.4.1 Layout Guidelines

The layout of the TMP61 is similar to that of a passive component. If the device is biased with a current source, the positive pin 2 is connected to the source, while the negative pin 1 is connected to ground. If the circuit is biased with a voltage source, and the device is placed on the lower side of the resistor divider, V– is connected to ground and V+ is connected to the output, V_{TEMP}. If the device is placed on the upper side of the divider, V+ is connected to the voltage source and V– is connected to the output voltage, V_{TEMP}.

8.4.2 Layout Example

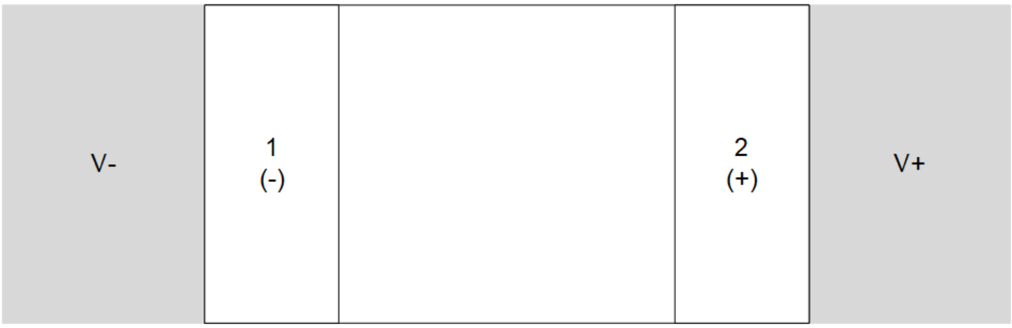


Figure 8-14. Recommended Layout: DEC Package

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.3 Trademarks

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9.4 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (February 2019) to Revision F (November 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Updated temperature support to 150°C	1
• Updated Description section	1
• Updated Device Comparison Table	2
• Added notes to pinout diagrams	3
• Changed minimum Junction Temperature from –40°C to –65°C in *Absolute Maximum Ratings table*	4
• Changed Max Storage Temperature from 150°C to 155°C in *Recommended Operating Conditions*	4
• Changed Max Ambient Temperature from 125 °C to 150 °C for DYA package in *Recommended Operating Conditions*	4
• Added 1000 hour Long Term Drift specification for DYA package	5
• Added LPG Thermal response	5
• Updated Typical Characteristics curves	6
• Moved the *Power Supply Recommendations* and *Layout* sections to the *Application and Implementation* section	16

Changes from Revision D (December 2019) to Revision E (February 2020)	Page
• Updated Features list	1
• Updated Applications list	1
• Updated Description	1
• Changed Maximum temperature of DEC package in Device Comparison Table from 150°C to 125°C	2
• Changed Max Junction Temperature from 150°C to 155°C in *Recommended Operating Conditions*	4
• Added 'Long Term Drift ' for DYA package	5
• Changed min spec 'Long Term Drift' for RH = 86 % from 0.1 % to -1 %	5

- Added typical spec 'Long Term Drift' for RH = 86 %.......5
- Changed max spec 'Long Term Drift' for RH = 86 % from 0.8 % to 1 %.......5
- Changed min spec 'Long Term Drift' for DEC package from 0.1 % to -1 %.......5
- Added typical spec 'Long Term Drift' for DEC package'.......5
- Changed max spec 'Long Term Drift' for RH = 86 % from 1 % to 1.8 %.......5
- Added typical spec 'Long Term Drift' for LPG package.......5
- Changed max spec 'Long Term Drift' for RH = 86 % from 1.1 % to 1.4 %.......5
- Updated Overview section.......8
- Added TMP61 R-T Table section.......9
- Updated Feature Description section.......9
- Removed Transfer Tables.......9
- Updated Application and implementation section to match TI data sheet standards.......10
- Added link to Thermistor Design tool.......10
- Removed Thermal Compensation section.......11

Changes from Revision C (September 2019) to Revision D (December 2019) **Page**

- Removed preview notice from the SOT-5X3 package.......1

Changes from Revision B (July 2019) to Revision C (September 2019) **Page**

- Added preview SOT-5X3 package.......1

Changes from Revision A (June 2019) to Revision B (July 2019) **Page**

- Changed *Application* bullets.......1
- Increased ESD CDM Rating.......4
- Removed 'Functional, Unspecified Performance' rows.......4
- Removed 'Functional, Unspecified Performance' rows.......4
- Added Thermal Information for LPG Package.......4
- Added 'Long Term Drift' spec for LPG package.......5
- Added transfer tables for the LPG package.......9
- Changed *Layout Example* section.......16

Changes from Revision * (December 2018) to Revision A (June 2019) **Page**

- Changed data sheet status from Production Mixed to Production Data.......1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMP6131DECR	Active	Production	X1SON (DEC) | 2	10000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EL
TMP6131DECR.A	Active	Production	X1SON (DEC) | 2	10000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	EL
TMP6131DYAR	Active	Production	SOT-5X3 (DYA) | 2	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	1GK
TMP6131DYAR.A	Active	Production	SOT-5X3 (DYA) | 2	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	1GK
TMP6131DYAT	Obsolete	Production	SOT-5X3 (DYA) | 2	-	-	Call TI	Call TI	-40 to 125	1GK
TMP6131LPGM	Active	Production	TO-92 (LPG) | 2	3000 | AMMO	Yes	SN	N/A for Pkg Type	-40 to 150	TMP61
TMP6131LPGM.A	Active	Production	TO-92 (LPG) | 2	3000 | AMMO	Yes	SN	N/A for Pkg Type	-40 to 150	TMP61

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF TMP61 :

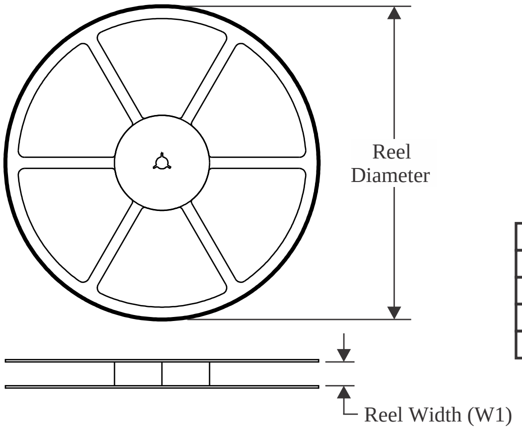
- Automotive : TMP61-Q1

NOTE: Qualified Version Definitions:

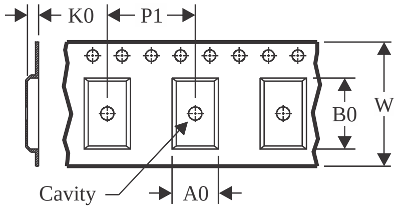
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

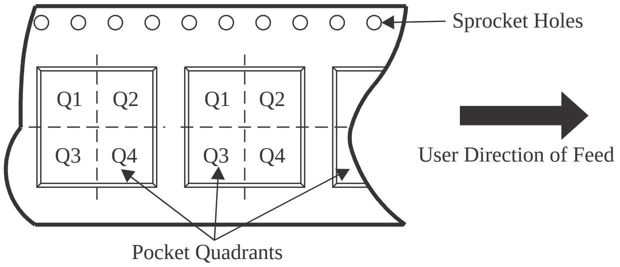


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

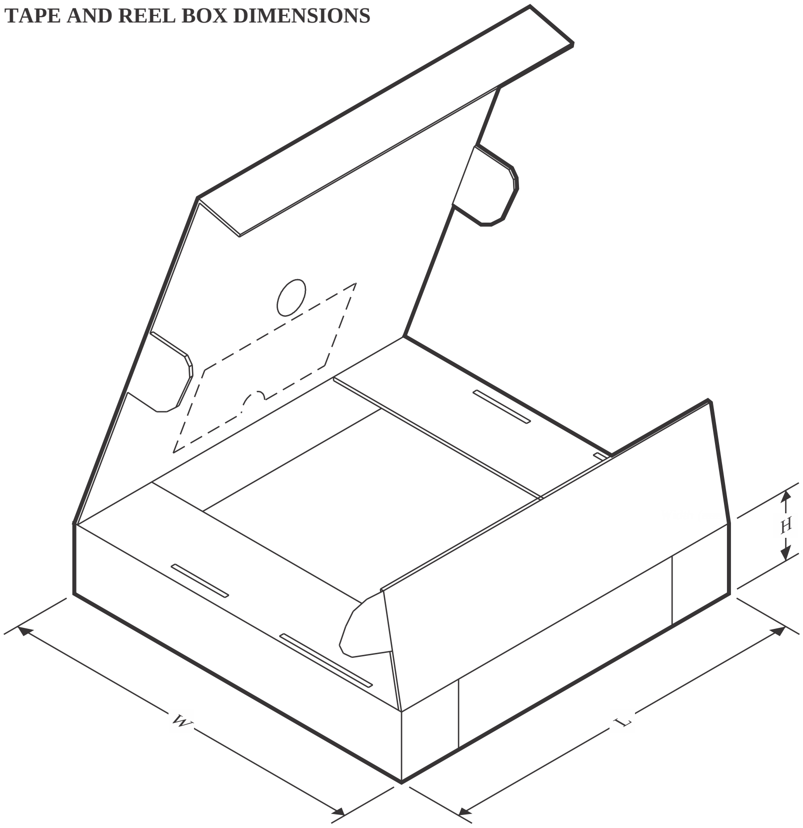
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP6131DECR	X1SON	DEC	2	10000	178.0	8.4	0.7	1.15	0.47	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



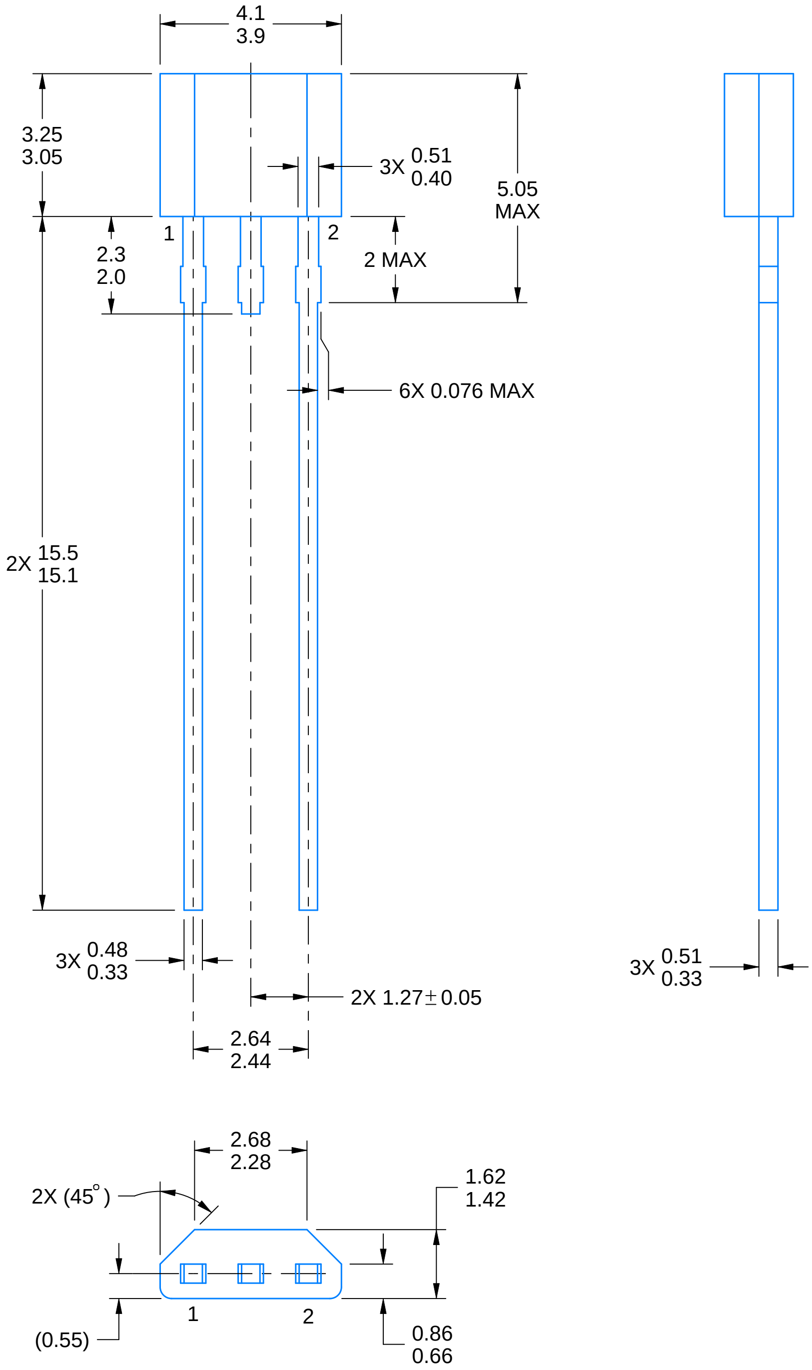
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP6131DECR	X1SON	DEC	2	10000	205.0	200.0	33.0

PACKAGE OUTLINE

TO-92 - 5.05 mm max height

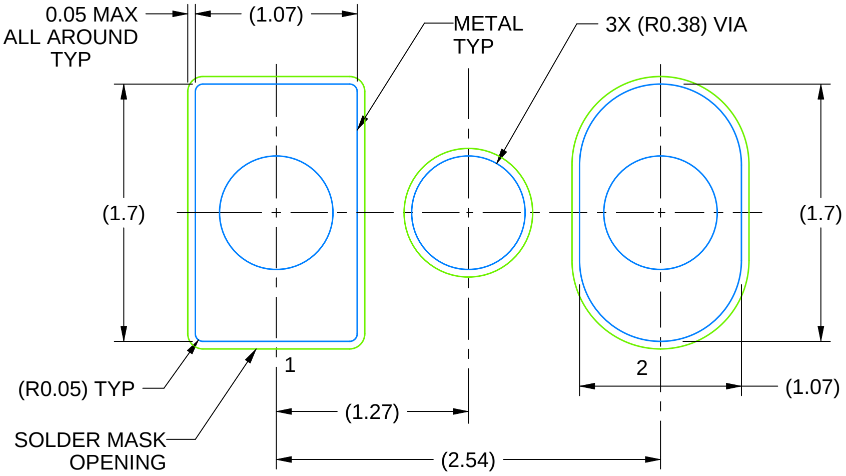
TRANSISTOR OUTLINE



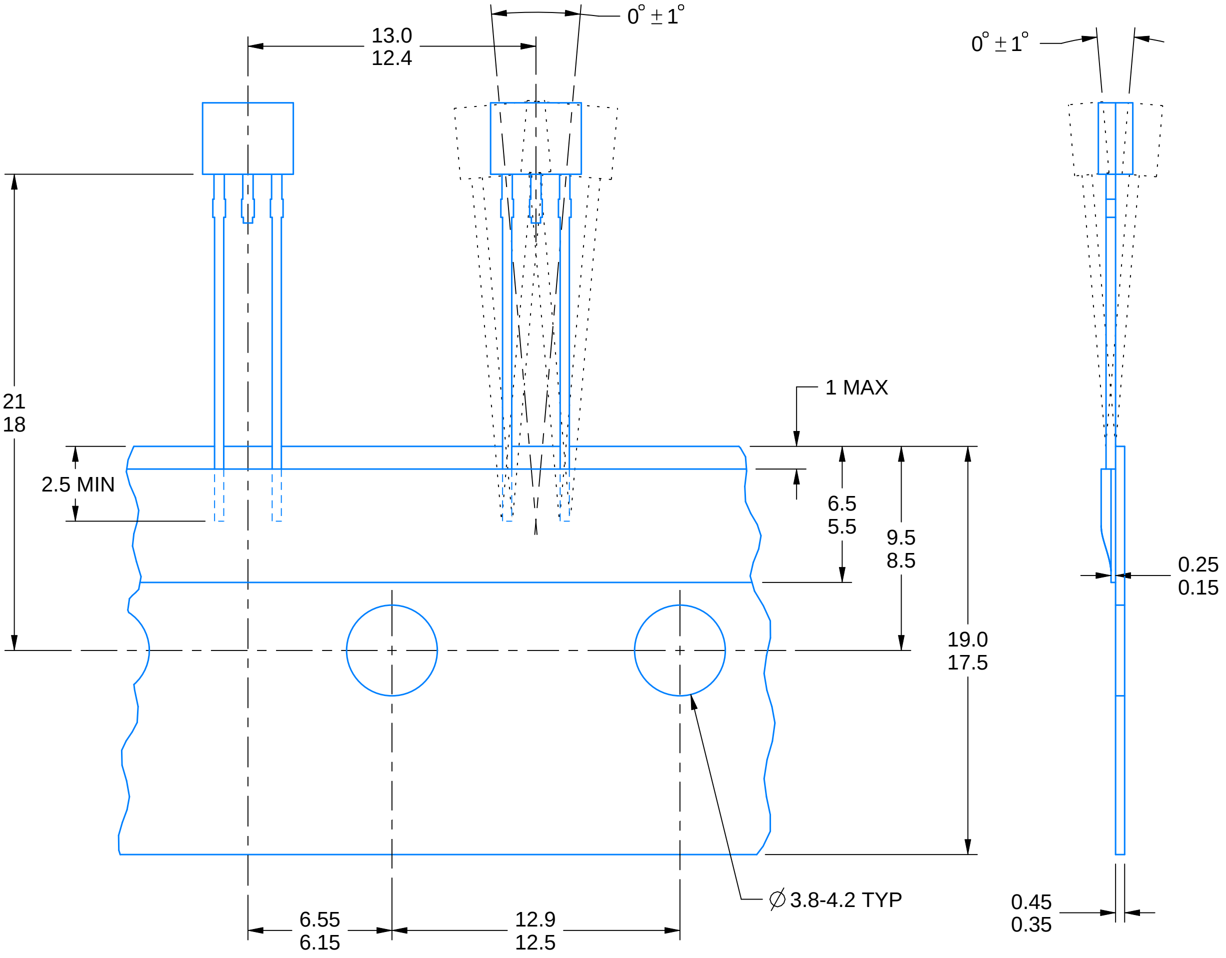
4221971/B 06/2022

NOTES:

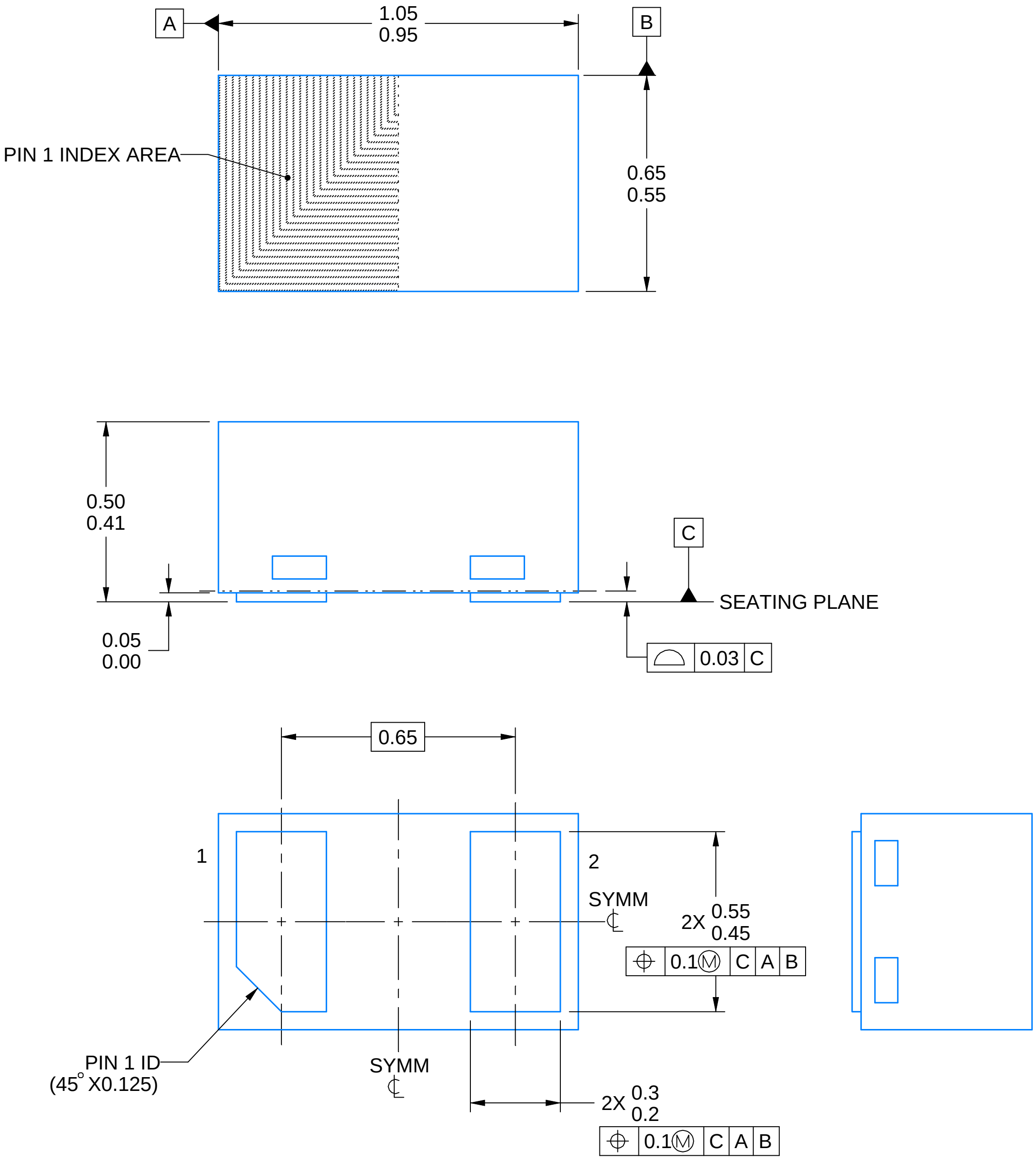
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:20X



4221971/B 06/2022

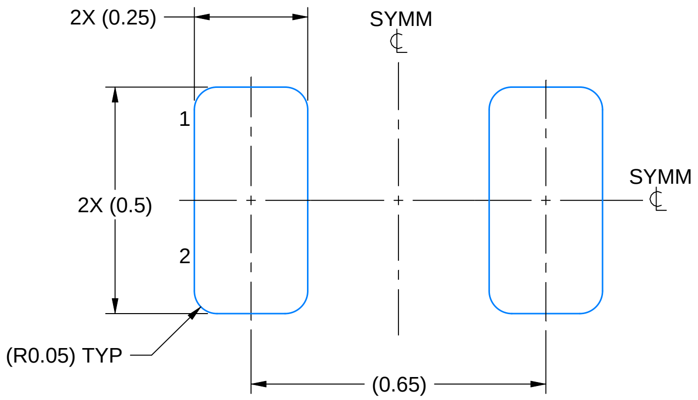


4224506/A 08/2018

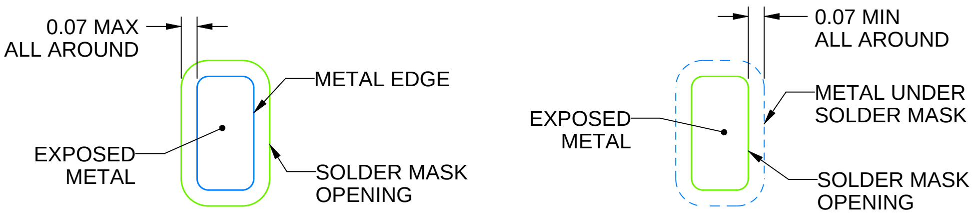
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X



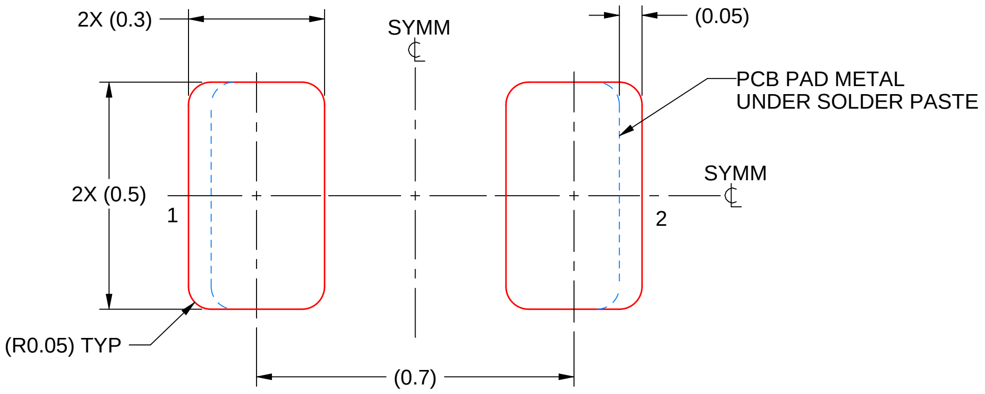
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK DETAILS

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

4224506/A 08/2018

NOTES: (continued)

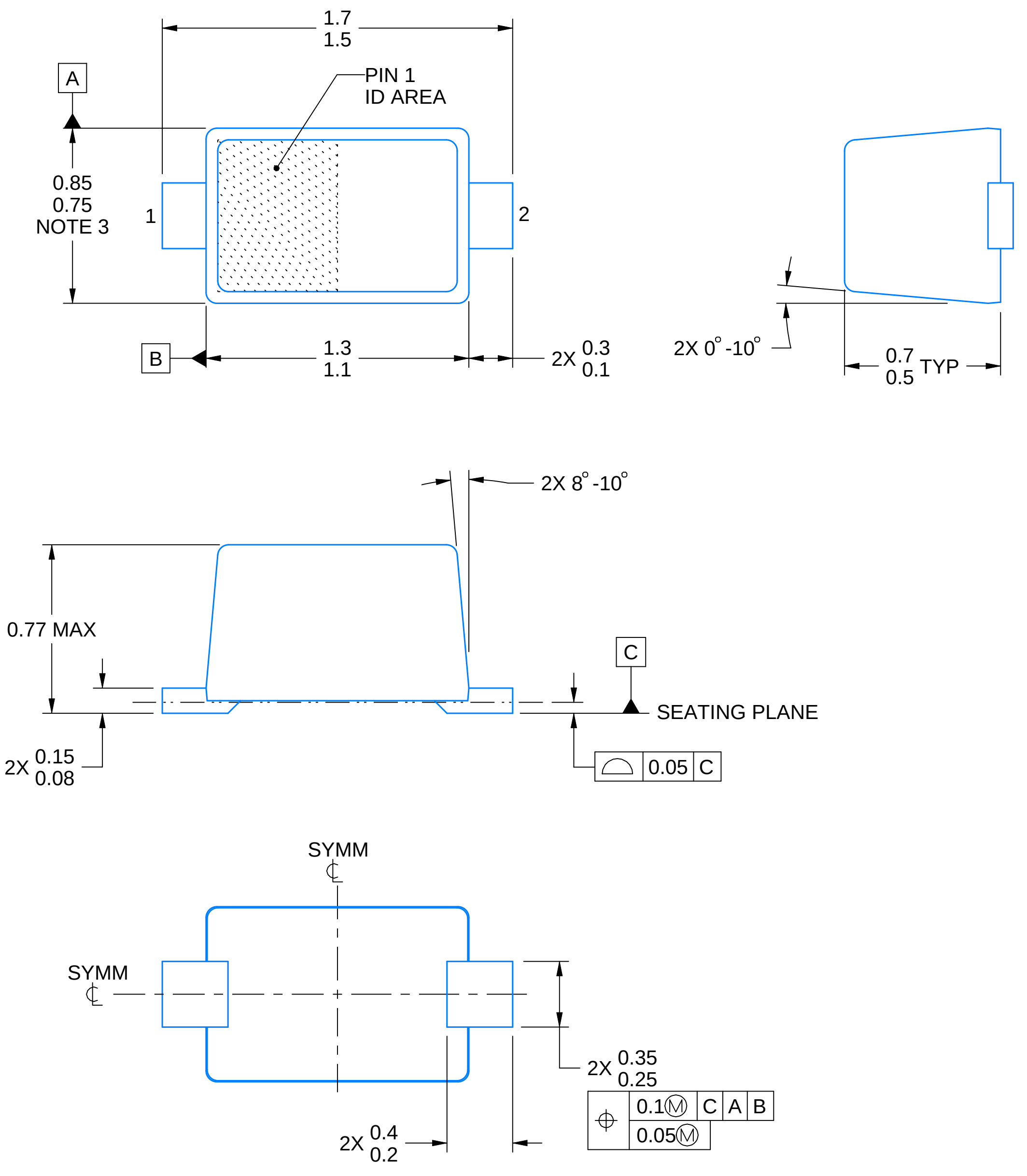
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DYA0002A

SOT (SOD-523) - 0.77 mm max height

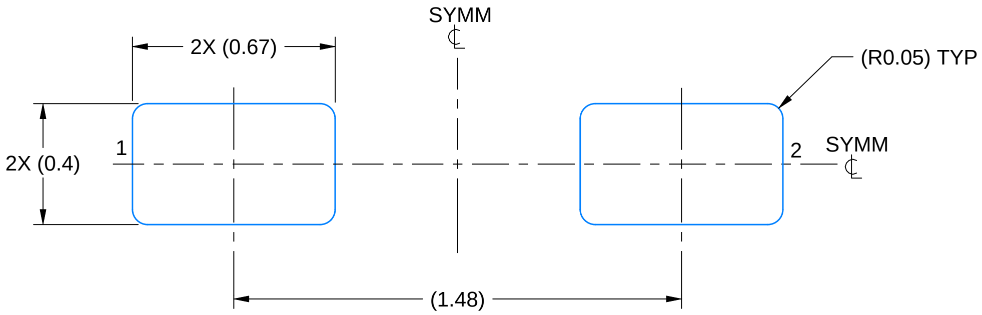
PLASTIC SMALL OUTLINE



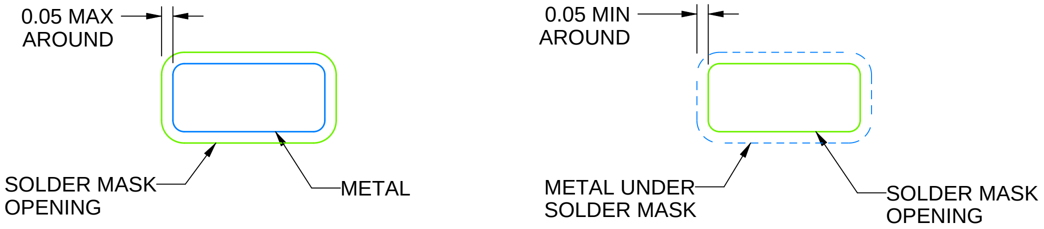
4224978/C 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEITA SC-79 registration except for package height



LAND PATTERN EXAMPLE
SCALE:40X



NON SOLDER MASK
DEFINED
(PREFERRED)

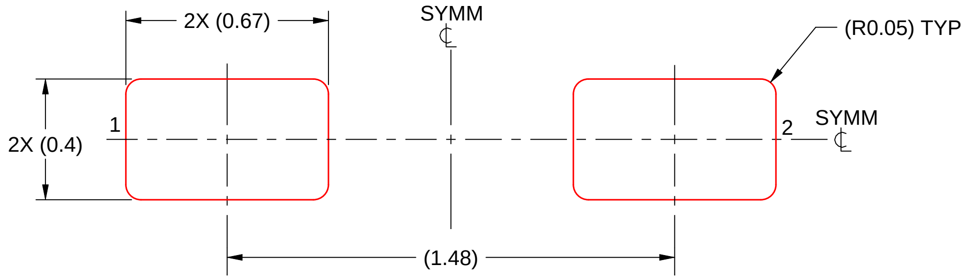
SOLDER MASK
DEFINED

SOLDERMASK DETAILS

4224978/C 11/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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